

### INFORMATION ON DOCTORAL THESIS

1. Full name : Đỗ Văn Chiêu ..... 2. Sex: Male.....

3. Date of birth: 19/08/1979 ..... 4. Place of birth: HaiPhong .....

5. Admission decision number: 4154/QĐ-SĐH Dated 15/07/2008

6. Changes in academic process:

Changed thesis title to “Formal method and specification of component interfaces with service quality and concurrency included”, decision number 201 /QĐ-ĐT, signed date: 09/04/2011.

7. Official thesis title: Formal method and specification of component interfaces with service quality and concurrency included.

8. Major: Software Engineering..... 9. Code: 62.48.01.03 .....

10. Supervisors: Dr. Đặng Văn Hưng and Assoc. Prof. Nguyễn Việt Hà

11. Summary of the **new findings** of the thesis:

The thesis proposes timed trace theory to support the specification of time constraints of real-time concurrent systems. Timed trace theory is a timed extension of Mazurkiewicz’s trace theory by using a timed labeling function. According to this extension, timed trace theory is effective to use in specifying behaviors of timed concurrent systems. In addition, the authors proposed a duration trace notion, duration trace is Mazurkiewicz trace that a character (an action) in dependent alphabet is labeled with a timed constraint, which is a timed interval. Duration trace is used in order to present timed constraints of systems in which each their action associates specification of the worst case execution time (WCET). Duration trace is a concise representation of a set of timed traces. The doctoral thesis included an asynchronous duration automaton to recognize the regular timed trace language in order to apply to verification problems. A result of this thesis is the emptiness checking problem of asynchronous duration automata to be decidable whether complexity is not polynomial. To support the specification of systems, in the timed trace theory, the thesis also included Timed Linear Temporal Logic (TLTL) to specify timed trace properties. This sort of logic is a timed extension of Linear Temporal Logic (LTL - Linear Temporal Logic). The association between asynchronous automata and TLTL has proposed and proved. Hence, together with above timed trace theory, timed concurrent systems will be conveniently specify and verify depending on asynchronous duration automata and TLTL fomulars.

The evidence of effectiveness of proposal methods, applies the method proposed in the specification, analysis and verification of component-based systems. For each model, all behaviors of system are specified by timed traces. Therefore, the model can specify concurrent properties and timed constraints of systems that need to verify.

- The first, the thesis introduce to a model component-based timed concurrent systems relying on rCOS (Refinement of Component and Object Systems). This research uses timed trace to specify interface protocols of component, the computations over compositional operators, and component refinement has proposed and proved.
- The second, the authors proposed a designing model based-on interfaces over timed concurrent systems. In this model, timed concurrent interface automata is used to model each component. The results showed that new methods can cover all other aspects of interface-based design theory.
- Finally, a new method is proposed to specify and specify timed concurrent distributed systems. The main idea is a widening of distributed transition systems, using timed trace language.

12. Practical applicability, if any: The results of the thesis can be applied in the interface modeling techniques in the theory of interfaces for component-based systems with time constraints and concurrency

13. Further research directions, if any: Applying theoretical research into a model checker tool, studying and optimal complexity of the verification algorithms proposed in the thesis.

14. Thesis-related publications: .....

- [1] Do Van Chieu and Dang Van Hung (2010), An extension of Mazurkiewicz traces and their applications in specification of real-time systems, In Proceedings of the second international Conference on knowledge and systems engineering 2010. IEEE Computer Society, pp. 167-172.
- [2] Do Van Chieu and Dang Van Hung (2011), A formal model for concurrent real-time component-based systems, Journal of science and technology Vietnam, Vol. 49, No.4A, pp. 313-226 (ISSN: 0866 708X).
- [3] Do Van Chieu and Dang Van Hung (2012), Timed traces and their applications in specification and verification of distributed real-time systems, In Proceedings of the Third International Symposium on Information and Communication Technology 2012, IEEE Computer Society, pp. 31-41.

[4] Do Van Chieu and Dang Van Hung (2015), A Formal Method for Specifying Interface of Component in Real-time Concurrent Systems, Journal of Information Communication Technology, Vietnam, Vol. E-3, No. 8(12), pp. 48-57 (ISSN: 1859 – 3534).

Date: 10/10/2015

**Signature of supervisors**

**Dang Van Hung**

Date: 10/10/2015

**Signature of PhD student**

**Do Van Chieu**